PROCESSOR CORE CLOCK GENERATION CIRCUITS

ABSTRACT OF THE DISCLOSURE

An invention is provided for generating custom clock frequencies within a processor core. A CPU clock signal propagates through a DLL circuit. Further, a control signal controls the CPU clock signal as the signals propagate through multiple inverters in the DLL circuit. The multiple inverters delay the CPU clock signal and generate multiple output signals. Subsequently, the multiple output signals are combined to generate a higher frequency signal than the CPU clock signal. To control the CPU clock signal, the DLL circuit includes a charge pump to lock in a precise control signal. The charge pump further includes circuitry, such as a Schmitt circuit, to increase and decrease voltage.